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SYSTEM OF DIGITAL DEVICE TEST GENERATION FOR ACTIVE HDL

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Abstract. *The models and methods for digital design analysis and test generation, where problems of digital design testing are formalized as linear equations, are offered. The method of test generation for stuck-at faults, which uses fault list cubic coverings (FLCC) for single activation path building, is developed. The ATPG for digital designs created in Active-HDL is offered as well. The obtained tests are used for digital design verification by means of simulation in Active-HDL.*

Key Words. *ATPG, Active HDL, FSM model.*

1. MATHEMATICAL APPARATUS FOR FSM MODEL ANALYSIS

Sequential primitive automatic model [1,2] is represented as follows:

$$M=<X, Y, Z, f, g>, \quad (1)$$

where $X=(X_1,X_2,...,X_i,...,X_m)$, $Y=(Y_1,Y_2,...,Y_i,...,X_h)$, $Z=(Z_1,Z_2,...,Z_i,...,Z_k)$ – are sets of input, internal and output State (FSM) variables, the interconnection of which is described by the following characteristic equations:

$$Y(t)=f[X(t-1), X(t), Y(t-1), Z(t-1)];$$
$$Z(t)=g[X(t-1), X(t), Y(t-1), Y(t), Z(t-1)]. \quad (2)$$

Variables Z(t) are external and, therefore, they are observed on output lines. Variables Y(t) are internal and, therefore, they are non-observed. FSM variables format for cubic covering, corresponding to (1), is as follows:

X(t−1)	Y(t−1)	Z(t−1)
X(t)	Y(t)	Z(t)

.

FSM model from Fig.1 corresponds to the mentioned format.

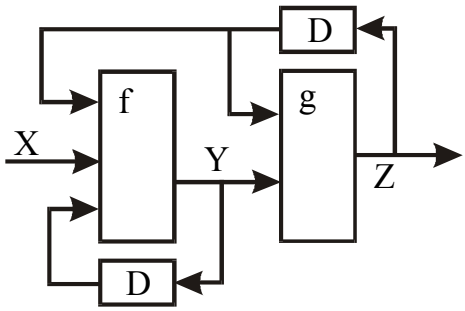

Fig.1. The primitive's state model

Functional sequential primitive is specified by components:

$$F^2 = <(t\text{-}1,t),(X,Z,Y),\{A^2\}>, \tag{3}$$

where (t-1,t) – are two state consecutive frames in function description; (X,Z,Y)– are vectors of input, internal and output variables; $\{A^2\}$ – is a two-frame alphabet of FSM state (transition) description:

A^2={Q=00,E=01,H=10,J=11,O={Q,H},I={E,J},A={Q,E},
B={H,J},S={Q,J},P={E,H},C={E,H,J},F={Q,H,J},L={Q,E,J}, V={Q,E,H},Y={Q,E,H,J},
A^1={0,1,X={0,1}}, (U)}.

Execution of the concatenation operation (#):

$$C_{t-1}\#C_t = \begin{array}{|c|c|c|c|}\hline \# & 0 & 1 & X \\ \hline 0 & Q & E & A \\ \hline 1 & H & J & B \\ \hline X & O & I & Y \\ \hline \end{array}. \tag{4}$$

Problem 1. FLCC L for the vector T and the primitive covering C is computed by a linear equation

$$T \oplus C = L, \tag{5}$$

where $\oplus$ – is a binary coordinate operation XOR which determines interaction of components T, C, L in the three-valued alphabet:

$$T_j \oplus C_{ij} = \begin{array}{|c|c|c|c|}\hline \oplus & 0 & 1 & X \\ \hline 0 & 0 & 1 & X \\ \hline 1 & 1 & 0 & X \\ \hline X & X & X & X \\ \hline \end{array}. \tag{6}$$

The universal formula of FLCC analysis obtained as a result of application of (3) to the test-vector T and to covering of the multioutput primitive C for definition of detectable faults Lr by output r, is as follows:

$$L = \bigcup_{\forall i(T_r \oplus C_{ir}=1)} \bigcap_{j=1}^{k} L_j^{T_j \oplus C_{ij}}, \qquad L_j^{T_j \oplus C_{ij}} = \begin{cases} L_j \leftarrow T_j \oplus C_{ij} = 1; \\ \bar{L}_j \leftarrow T_j \oplus C_{ij} = 0, \end{cases} \tag{7}$$

where $\bar{L}_j$ – is considered as a line j fault list that should be subtracted from faults which are detected at non-output primitive lines; L_j – are faults that are required to be intersected with non-output lists.

Problem 2. Test for FSM faults, which are set by L_i^1-cube from FLCC $L = (L_i^0, L_i^1)$, is defined by equation

$$L_i^1 \oplus C = T^k \tag{8}$$

where L_i^0, L_i^1 - are cubes having "0" or "1" values on output coordinate r. At the same time vectors-candidates to test $T_t^k \in T^k$ are defined. From set T^k the test T is formed, where the set $T_t \in T$ is regarded as an element. Each $T_t \in T$ must fulfil conditions:

$$T_t = C_i \cap T_t^k \Leftarrow \exists i(C_i \cap T_t^k \neq \varnothing) \tag{9}$$

2. ATPG SYSTEM

Purpose of automatic test pattern generator (ATPG) creation is verification of digital designs in Active-HDL system, which later will be implemented in Field Programmable Gate Array (FPGA), Complex Programmable Logic Device (CPLD), which are on one level with general matrix chips and signal processors now.

ATPG system solves the following tasks:

1. Test generation for FSM represented by transition graph. Representative languages are VHDL, Verilog.

2. Test generation for digital designs projects represented by Boolean equations. Representative language is VHDL.

3. Evaluation of test quality by single stuck-at- fault simulation.

2.1. The structure of TESTBUILDER program

The program is intended for automatic test generation with respect to single stuck-at faults of digital designs, which are described in language of Boolean equations.

Program operations:

1. Pseudo-random test generation in term of built-in binary code generators and decimal code generators.

2. Deterministic binary test-vector generation, where the mentioned test-vectors activate single logical paths in circuit.

3. Single stuck-at fault simulation [1] with purposes of evaluation of fault coverage of obtained test.

4. Test formatting in standard of VHDL - Testbench.

As an example of test building for circuit (Fig. 2) the following result is given:

Test =

No	012345	%
1 – Vector	01X010	
Faults =	10.101	41.67
Total =	10.101	41.67
2 – Vector	100000	
Faults =	1X1101	58.33
Total =	1X1101	58.33
3 – Vector	11X111	
Faults =	00.000	41.67
Total =	XX1X0X	83.33
4 – Vector	X01001	
Faults =	0000X0	58.33
Total =	XXXXXX	100.00

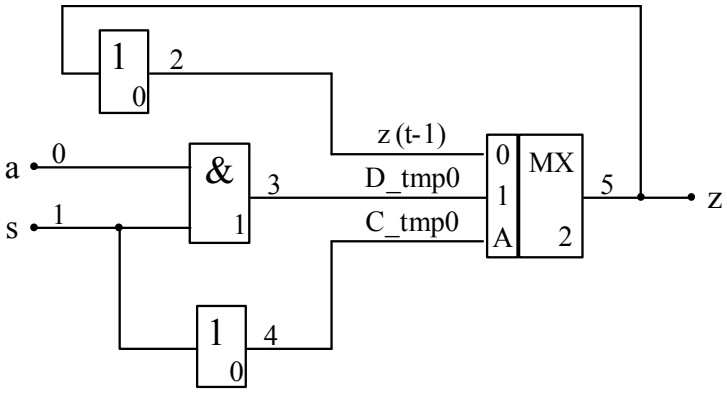

Fig. 2. Example of digital circuit

The program has processed:

- 10 combinational circuits from list ISCAS'85;
- 140 combinational and sequential circuits from PRUS; 45 sequential circuits with large complexity from PRUS;
- 22 sequential circuits from list ITC'99; average time of deterministic test generation is 2 hours.

Average complexity of design is 1000 lines. Average time of pseudo-random test generation is 5 minutes. Test coverage is more than 90 %.

CONCLUSIONS

The proposed models and methods are realised in the form of program applications. The last ones are used for test generation of digital designs based on FPGA and CPLD. The class of evaluated structures is the FSM in the form of transition graph and Boolean equations with flip-flop circuit. Digital circuit description language is VHDL. Program applications are directed toward their use in CAD systems: Aldec, Xilinx.

REFERENCES

[1] Hahanov V.I., *Cubic fault simulation and test generation for digital circuits*, Annual report of KTURE, 1999-2000, pp.139 - 146

[2] Hahanov V.I., KoKovalyov EE.V., Hanko V.V., Mehedi M.M., "Test generation system for FSM designing in ACTIVE-HDL", *ACS and automaton devices*, KTURE, Kharkov, №.111, pp.5-22.

[3] Bondarenko M.F., Krivoulya G.F., Riabtcev V.G., Fradkov S.A., Hahanov V.I., *Designing and diagnosis of computer systems and networks*, K.: SMC HE. 2000, 306 p.