The International Workshop
on Discrete-Event System Design, DESDes'01,
June 27÷29, 2001; Przytok near Zielona Gora, Poland

BENEFITS OF HARDWARE ACCELERATED SIMULATION

Remigiusz WIŚNIEWSKI, Arkadiusz BUKOWIEC, Marek WĘGRZYN

Computer Engineering and Electronics Institute, Technical University of Zielona Góra,
ul. Podgórna 50, 65-246 Zielona Góra, POLAND,
R.Wisniewski@cookie.iie.pz.zgora.pl, A.Bukowiec@cookie.iie.pz.zgora.pl,
M.Wegrzyn@iie.pz.zgora.pl

Abstract. *Today's sophisticated digital designs are rapidly evolving. Software-only simulation of such designs takes weeks or even months. Therefore a new generation of chip design requires a hardware-assisted solution. Hardware acceleration delivers a 10-1000 times performance boost. In the paper technologies of hardware simulation on selected examples are described.*

Key Words: *HDL, design verification, simulation, hardware acceleration, PLI*

1. INTRODUCTION

The designs are rapidly evolving, doubling in size with each generation and heading to tens million gates by 2002. This causes dramatic increase of the simulation run time. It is harder and harder to simulate designs because the simulation time has increased from minutes and hours to days and weeks. Therefore, the days of being able to verify ASICs and system-on-a-chip (SoC) designs through software-only simulation are over. Simulation assisted by special hardware is the best solution for speeding up the simulation of large design sections that have been tested and accepted by RTL simulations.

In the paper the three selected examples of hardware simulators are discussed. In addition, an analysis of software-only and hardware accelerated simulation of example complex design is described.

2. DESIGN VERIFICATION

A verification of SoC was time consuming because there were no fast RTL simulators and easy to use hardware emulators. The existing hardware accelerators for gate level design verification require extensive set-ups, good design understanding, lengthy compilations and tedious design partitioning into multiple FPGA devices. Companies involved in large SoC designs with critical time-to-market demands use this technology. It is not for the entry-level designers working with a limited budget.

The new RTL code hardware accelerators hold some promise but it is alleged that they involve lengthy compilations. They also do handle neither mixed VHDL/Verilog, nor very

large designs. Also, some IP cores come in EDIF or other proprietary formats and they need to be simulated outside those RTL accelerators. Until now there hasn't been a simple and universal tool or method that would accelerate verification of both RTL code and netlist-based (gate level) IP cores [10].

Figure 1 shows current design prototyping process [12]. At the beginning a designer prepares module *A* that is verified in simulator. Then he can create module *B*. When module *B* is ready, it is verified as a separate module and then with the rest of the design, and so on. This process is called also incremental prototyping. However the described process takes hours and even days. Current designs consists of several millions gates, so the simulation takes too much time. Therefore CAD companies introduced new technology – hardware accelerated simulation.

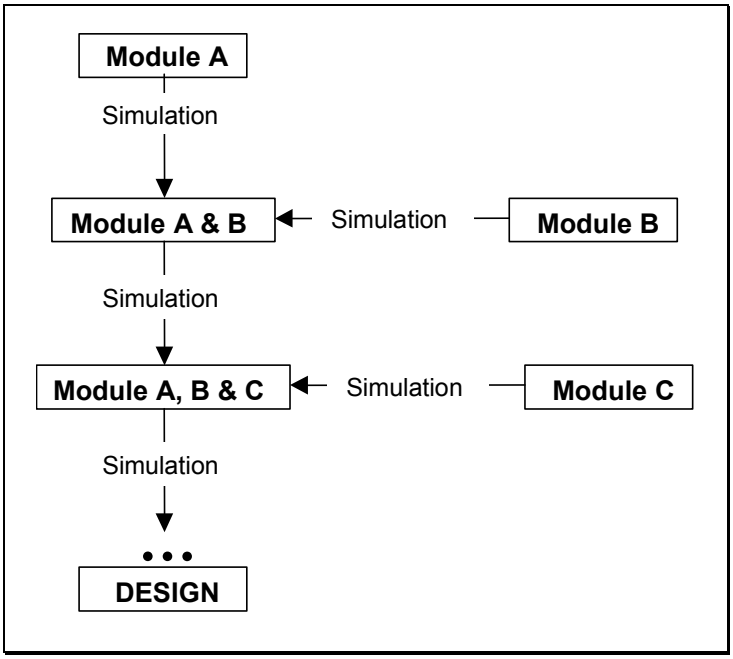

Fig. 1. Current design verification process

3. HARDWARE ACCELERATED SIMULATION TECHNOLOGY

Hardware simulation is a technology that allows speed up simulation time, turning weeks or months of simulation into days or even hours. Designer can "push" whole or a part of the design into hardware. Because it is rather a new technology every solution is different and has different features. Some vendors produce only hardware simulators, others manufacture hardware and also software simulators.

3.1. Xcite-2000 (Axis Systems, Inc.)

Xcite-2000 [3] is the simulation acceleration technology. Xcite-2000 preserves the native simulation-debugging environment. With its Re-Configurable Computing (RCC) technology, Xcite-2000 offers simulation performance up to 100K cycles/second on a design capacity up to 10 million ASIC gates.

Transparent Simulation access to RCC Architecture for Xcite-2000 integrates software and hardware into one unified package. The hardware contains a Re-Configurable Computer (RCC) composed of the Altera FPGA Flex [2]. Xcite-2000 RCC directly connects with the workstation via one set of PCI extender. Whether the system design is described at the

behavioural, RTL or gate level, the Xcite-2000 compiler custom configures its computing elements to maximize parallel processing. Thus, design simulation with Xcite-2000 is identical to software simulation at hardware speed.

Design description can be separated into three components: behavioural, RTL and gates. The Xcite compiler automatically maps sections, which can be RCC accelerated (RTL and gate level components) and builds a native compiled simulation image for behavioural sections, which need to stay within the Axis software simulator, Xsim. Using "Hierarchy Extracted" mapping technique, the Xcite compiler automatically maps the design onto arrays of FPGAs.

One of the unique capabilities of Xcite-2000 is its ability to swap software and RCC state in real time. Thus during simulation, the user may choose to swap all RCC state into Xsim in order to debug the design and continue software simulation. Once the circuit is fully diagnosed, simulation state value can be swapped back into RCC for maximum performance acceleration.

Within Xcite RCC simulation, simulation history for all nodes is compressed within RCC and stored onto the workstation. Either during or after simulation, the Xcite VCD-on-Demand capability can extract all node history values without re-simulation. Thus design debugging has become highly efficient without the high cost of disk storage or simulation slowdown.

3.2. Viking CSM (IKOS Systems, Inc.)

The Viking CSM [5] co-simulator offers hardware accelerated simulation performance for verification of VHDL designs on the ModelSim software simulator from Model Technology, (MTI) [7]. The Viking CSM system delivers mixed-level acceleration through a tight integration of the ModelSim software with the NSIM and ARES hardware accelerators from IKOS.

Users work with their existing verification environment, workflow and language, using the same simulation test-benches to accelerate their designs. Viking CSM extends the command set and GUI capabilities of ModelSim's to support IKOS' accelerators. The product also allows the Foreign Language Interface (FLI) to ensure that Viking CSM will integrate properly with the user's systems and all peripheral tools.

Viking CSM offers also designers access to the debug capabilities of ModelSim without having to switch between different software and hardware environments.

The NSIM is an event-based hardware accelerator. This proven technology is based on a massively parallel, hyper-cube architecture optimised for event-driven simulation. Large designs are automatically partitioned across parallel custom simulation processors or "clusters" to achieve the accelerated speeds. ARES is a very affordable desktop accelerator based on the proven NSIM architecture, but is optimised specifically for RTL acceleration and comes bundled with software.

3.3. Hardware Embedded Simulation (Aldec, Inc.)

Hardware Embedded Simulation (HES) [1] is the technology that facilitates the incremental design verification of FPGA and ASIC devices while speeding up design verification. HES technology allows you to download selected modules of your design into an FPGA and perform hardware-software co-simulation. After a design block has been verified at the behavioral level, it is synthesized, implemented and downloaded into an FPGA residing on an accelerator board. HES technology supports up to four acceleration boards residing in one computer. The boards are the PCI cards inserted into the slots of the computer.

The entire design is simulated in the HES environment, which consists of an HDL software simulator and PCI boards. This environment assures correct communication between modules located in silicon and modules simulated in software.

Using the HES technology, verified modules of the design can be put into silicon after the synthesis of even a small part of the design. User needs to synthesize the modules that should be pushed into silicon, and the HES Design Verification Manager (DVM) will help to configure HES environment.

Aldec's simulator is based on the Incremental Prototyping. Figure 2 shows the idea of Incremental Prototyping. When module *A* is finished, it is synthesized and implemented and finally downloaded to the HES board. Since module *A* resides in the hardware simulator, the designer can prototype module *B* in software. When module *B* is verified successfully at the software level, it goes thru incremental synthesis and incremental place and route processes. Note that since module *A* now resides in the hardware, it is not synthesized and implemented again.

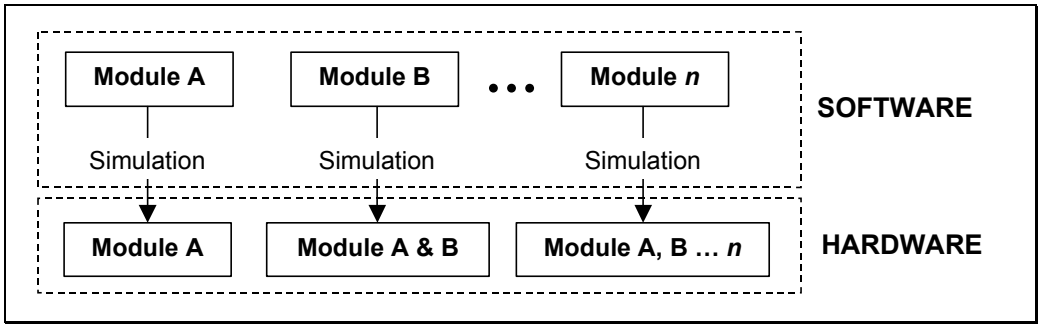

Fig. 2. Hardware acceerated design simulation process

HES boards have been built with Xilinx FPGA Virtex [11] or Altera CPLD Apex [2] devices. They are placed on the PCI board that can be put into the slot of the PC or Sun computer.

Aldec's hardware simulator works on the following platforms and configurations:

- Solaris (Sun) with MTI, Cadence [4], or Riviera simulators [1];
- Linux/Unix (PC) with Cadence, or Riviera simulators;
- Windows NT/2000 (PC) with MTI, or Active-HDL simulators [1].

3.4. Summary

Table 1 shows the summary of the selected hardware accelerators. Information about other solutions is described, for example, on [5,11].

Table 1. Summary of hardware accelerator

Feature	***HES***	***Xcite-2000***	***Viking CMS***
Real simulation	YES	YES	YES
Maximum Capacity	2,5 mln gates	1 mln gates	?
Used Chip(s)	Xilinx – Virtex Altera - Apex	Altera - Flex	Xilinx – Virtex
Supported Languages	Verilog, VHDL, EDIF netlist	Verilog	VHDL
Supported Simulators	Active-HDL, Riviera, ModelSim, Verilog XL/ NC-Sim	Xsim	ModelSim
Platforms	PC, SUN	SUN	SUN
Supported Operating Systems	Windows, Linux, Solaris	Solaris	Solaris

4. DESIGN EXAMPLE

This section shows the benefits of hardware simulation. The following results are based on a comparison between software and hardware simulation. The following example is based on using Aldec's software simulator (Active-HDL) and hardware accelerator board (Hardware Embedded Simulation - HES).

As an example a system consisted of two processors *MASTER* and *SLAVE* (Fig. 3). The design is a part of a bigger, hypothetical digital system, where data are processed in various ways. The purpose of these blocks is to process input data, and subsequently to send the result of processing to another module. The way that data are processed is not important for considered analysis. Since data can be transmitted from one module to another in an encrypted format, the design must be able to decrypt encrypted data. The first part (*MASTER* block) is responsible for data processing and communication with the rest of the system. The second part (*SLAVE* block) is responsible only for data encryption and decryption. Both blocks are modelled in Verilog-HDL [6]. Programming Language Interface (PLI) [8], a part of Verilog 1364-1995 standard (or a new, updated version – Verilog 1364-2001) is used for implementation of data exchange between the hardware and the software.

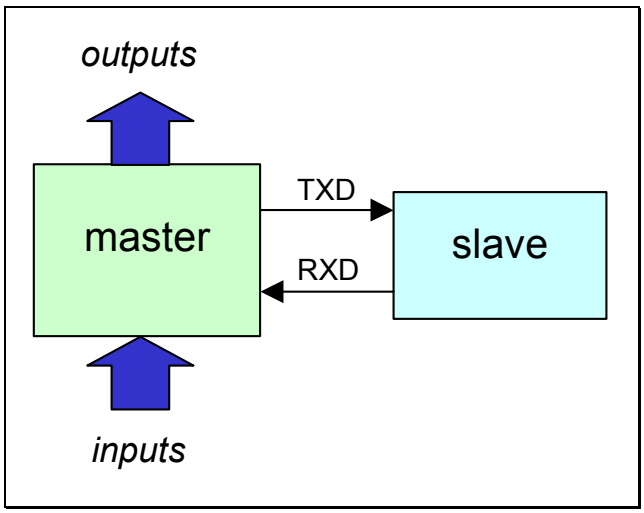

Fig. 3. Block diagram of an example system

When the *MASTER* block of the design is ready it is verified in software. The software verification of this Master block takes approximately 45 minutes. Next the *SLAVE* block is developed in software and also verified. The verification of the *SLAVE* block takes approximately 30 minutes. Verification of entire design is completed in approximately one hour and 15 minutes. Now if the design is not working properly it should be corrected and re-verified, repeating the entire cycle over again until the design is correctly verified in software. Conversely, this reiterative process can take weeks or even months.

Using HES hardware, the *MASTER* block is "pushed" into hardware after correct software verification. When the verification process is run again, the *MASTER* block will now simulate and verify in approximately 15 seconds versus 45 minutes. Next the *SLAVE* block is developed in software. Simulation and verification of this block takes 30 minutes in software. But when simulation and verification of both blocks is run again, verification of the entire design is completed in 30 minutes and 15 seconds. There is a noticeable decrease in time due to the *MASTER* block residing in hardware. Once the *SLAVE* block is verified correctly in software, it is "pushed" into the hardware, as well. The two blocks now reside in hardware.

The next simulation of the two blocks takes place in hardware, and the whole design is completed in 25 seconds (15 seconds for the *MASTER* and 10 seconds for the *SLAVE* block).

Table 2 shows times of hardware and software simulation for the considered design.

Table 2. Hardware vs. software simulation

Part of system	*Software simulation [min]*	*Hardware accelerated simulation [sec]*	*Software vs. Hardware [times]*
1. Master Block	45	17	159
2. Slave Block	30	10	180
3. The whole system	75	27	167

5. SUMMARY

Present digital designs are bigger and bigger. Very often simulation of such designs takes not only minutes and hours, but whole days or even weeks. The best solution for this problem seems to be hardware accelerated simulation. After finishing the design at the RTL level, a user can push it into a real device and do simulation or emulation of the design.

Hardware acceleration delivers a 10-1000 times performance boost. In the paper a comparison between only three representative examples of hardware accelerations has been presented. Advantage of such approach for system verification has been described on an example of a system that consists of master and slave processors.

REFERENCES

[1] Aldec, Inc., *http://www.aldec.com*

[2] Altera, Inc., *http://www.altera.com*

[3] Axis Systems, Inc., *http://www.axiscorp.com*

[4] Cadence Design Systems, Inc., *http://www.cadence.com*

[5] IKOS Systems, Inc., *http://www.ikos.com*

[6] Institute of Electrical and Electronics Engineers, *IEEE standard 1364-1995 „IEEE Standard Hardware Description Language Based on the Verilog Hardware Description Language"*, New York, 1996

[7] Model Technology, Inc., *http://www.modelsim.com*

[8] S.Mittra, *Principles of Verilog PLI*, Kluwer Academic Publishers, Norwell, 1999

[9] Quickturn, *http://www.quickturn.com*

[10] M.J.S.Smith, *Application-Specific Integrated Circuits*, Addison-Wesley, Boston, 1997

[11] Tharas Systems, *http://www.tharas.com*

[12] Xilinx, Inc., *http://www.xilinx.com*

[13] M.Zwoliński, *Digital System Design with VHDL*, Prentice Hall, Harlow (England), 2000